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10/639,350	08/12/2003	Robert M. Crosby	TI-34618	6171

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2112	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/639,350	CROSBY, ROBERT M.	
	Examiner	Art Unit	
	ESAW T. ABRAHAM	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 November 2007*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7-10 and 14-17* is/are pending in the application.

4a) Of the above claim(s) *5, 6 and 11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7-10 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Applicant's Response/Amendment

The drawings (Replacement Drawing sheets) were received on 11/19/07. These drawing are accepted.

In view of the amendment filed on 11/19/07, the Examiner withdraws all objections to the claims.

In view of the applicant's argument filed on 11/19/07, the Examiner withdraws 112, 2nd rejections to the claims.

Applicants are requested to cancel non-elected claims 5, 6, and 11-13 in subsequent communication.

Response to Amendment

Applicant's arguments with respect to claims 1, 3, 4, 7-10 have been considered but are not persuasive and further the claims are rejected in view of the new ground(s) of rejection.

Detailed action

1. Claims 1, 3, 4 and 7-10 and 14-17 remain pending.

2. Claim 2 is cancelled.

DRAWINGS

3. The drawings are objected to because:

- In figure 2, reference number 225 refers to "BIT UNIT" and in the specification (i.e., page 5 line 22 and 23) reference number 225 refers to "bit correction unit",

reference number 221 refers to "erase condition valid flag" and in the specification (i.e., page 5 line 27) reference number 221 refers to "bit correction unit" and reference number 226 refers to "interrupt request flag unit" and in the specification (i.e., page 6 line 3) reference number 226 refers to "interrupt request unit". Applicant is suggested to check specification to make certain that it is consistent with the figures to avoid unnecessary confusion.

A proposed drawing correction or corrected drawings are required in reply to the office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Corrected drawings sheets in compliance with 37 CFR 1.121(d) are required in reply to the office action should include all the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended". If a drawing figure is to be cancelled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheet may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header so as not to obstruct any portion of the drawing figures. If the changes are not acceptable by the examiner, the applicant will be notified and informed of any required corrective action in the next office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to because:

On page 7, line 3 the period next to the phrase "signal group has an error." should be removed.

On page 7, line 4 the phrase "when error is detected I step 33" should be replaced to read as "When error is detected in step 33".

On page 5, line 26 "the erased conditioned valid 221" should match "the erased condition valid signal 221" on page 6 line 7 for the purpose of uniformity of the terms.

On page 6, line 3 "the interrupt request flag unit" 226" should match "the interrupt request unit 226" on page 6 line 3 for the purpose of uniformity of the terms.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Claim objections

5. Claim 14 is objected because of the following informalities:

In line 3, the claim recites, "A non-volatile error memory" and it should recite, "A non-volatile error checking and correction memory" to show proper antecedent.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 3, 4, 7-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. See MPEP 706.03(0). Amended independent claim 1 recites, "...wherein the error checking and correction unit includes circuitry for requesting an interrupt and/or for setting a flag which is polled, when a memory location of a failing bit is correctable".

The Examiner would like to point out that the specification (see for example, in the applicant's remark page 11, the applicant argues that, "When the central processing unit can be interrupted, the central processing unit restores the location in main memory where the error originated based on the stored address and location") and furthermore, specification on page 5, lines 9-17 only teaches "*When in step 34 the detected error is correctable, then the syndrome bits are calculated in step 35. In step 36, a determination is made whether the error is consistent with a failing bit in the main memory. When the detected failing bit is not consistent with a failing bit location in the main memory, then the erroneous bit is corrected in step 37 and the process returned to step 31 for execution of the program. When, in step 36, the detected error is consistent with a failing bit location, then the address of the signal group in which the error was detected and the correction pattern are stored in step 38. In step 39, an interrupt flag is set. The procedure then corrects the error and returns to step 31. In step 40, the interrupt flag is serviced by the central processing unit. The charge on the*

failing bit location is restored and the process returns to step 31" does not teach a circuitry for requesting an interrupt and/or for setting a flag which is polled, when **a memory location of a failing bit is correctable**.

Amended independent claim 7 recites, "... a failing bit apparatus, the failing bit apparatus identifying when a correctable error is the result of a failing bit memory location". The Examiner would like to point out that the specification does not teach a failing bit apparatus, the failing bit apparatus identifying when **a correctable error is the result of a failing bit memory location.**

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the present invention relates to the correction of the storage element itself in which the error signal is generated by reason of a failing bit and further the applicant contends that a variety of failing bits memory locations in the prior art and the present disclosure discusses only failing bit locations in **non-volatile memory locations**) (see independent claim 1 and claims that depend on claim 1) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claims **3, 4 and 8-10** depend from claims 1 and 7 are rejected under 35 USC 112, 1st paragraph for similar reasons.

Claim Rejections - 35 USC § 112, 2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 7 and 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites “error checking and correction unit”. It is not clear if the "error checking and correction unit” is referring to the “check calculation unit" (123) or "BIT UNIT” (225) or “error checking and correction memory” (122) of figure 2 and further the specification does not specifically teach or describe “the error checking and correction unit”. Clarification is required.

Claim 7 recites “error checking and correction apparatus”. It is not clear if the "error checking and correction apparatus” is referring to the “check calculation unit" (123) or "BIT UNIT” (225) of figure 2 and further the specification does not specifically teach or describe “the error checking and correction unit”. Clarification is required.

Claim 7 recites “a failing bit apparatus”. It is not clear if the "failing bit apparatus” is referring to the “check calculation unit" (123) or "BIT UNIT” (225) of figure 2 and further the specification does not specifically teach or describe “the error checking and correction unit”. Clarification is required.

Claim 15 recites the limitation "the failing bit memory location" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites “the error checking and correction code memory” which is inconsistent with what was previously recited (i.e. “the error checking and correction memory”): therefore, the recitation lack an antecedent basis (see line 10 and 11).

8. Claims **1 and 8** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

The omitted structural cooperative relationships are (in claim 1): error checking and correction unit" and circuitry". It is not clear where in the claimed error checking and correction unit said circuitry are exactly located. It is not clear if the circuitry is confined inside the error checking and correction unit or are exactly connected to the same. The interconnection of such elements can neither be visualized in the drawings nor can be clearly understood from the claimed language for proper examination.

The omitted structural cooperative relationships are (in claim 8): "failing bit apparatus" and all the three components such as address storage unit, an interrupt flag unit and correction pattern unit. . It is not clear where in the claimed failing bit apparatus said address storage unit, an interrupt flag unit and correction pattern unit are exactly located. It is not clear if the said address storage unit, an interrupt flag unit and correction pattern unit are confined inside failing bit apparatus or are exactly connected to the same. The interconnection of such elements can neither be visualized in the drawings nor can be clearly understood from the claimed language for proper examination.

Clarification is required.

Claims **3, 4 and 8-10** depend from claims 1 and 7 are rejected under 35 USC 112, 2nd paragraph for similar reasons.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims **1, 3, 4, 7-10 and 14-17** are rejected under 35 U.S.C. **102(b)** as being clearly anticipated by Abdoo et al. (hereafter referred to as Abdoo) (U.S. PN: 5,490,155).

As per claim 1:

Abdoo substantially teaches or discloses a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11). Abdoo further in figure 1 discloses the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22). Furthermore, Abdoo teaches signals such as (CERR signal and the NCERR signal) which controls the interrupts to the various CPUs in the computer system (see col. 11, lines 62-67) and when either the CERR signal or the NCERR signal is asserted, the

syndrome bits are stored in a diagnostic resister in the SDB (44, 45) that generated them. The register includes a series of other diagnostic bits, including a bit, which indicates whether the error occurred during a read cycle or a read-merge-write cycle (registers to hold the location of one or more bits). Furthermore,

Abdoo substantially teaches or discloses that when an error occurs, the computer system stores various data regarding the error so that the cause of the error may be analyzed. Both the CERR signal and the NCERR signal are provided to the CSP (46), which controls the interrupts to the various CPUs in the computer system. If the CERR signal is asserted, the CSP (46) asserts an interrupt request (IRQ) signal, indicating that a correctable error has occurred (see col. 11, lines 62-67).

As per claims 3-4:

Abdoo substantially teaches or discloses that when an error occurs, the computer system stores various data regarding the error so that the cause of the error may be analyzed. Both the CERR signal and the NCERR signal are provided to the CSP (46), which controls the interrupts to the various CPUs in the computer system. If the CERR signal is asserted, the CSP (46) asserts an interrupt request (IRQ) signal, indicating that a correctable error has occurred (see col. 11, lines 62-67).

As per claims 7 and 8:

Abdoo substantially teaches or discloses a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11). Abdoo further in figure 1 discloses that the computer

system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block (a failing bit apparatus) referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22). Furthermore, Abdoo teaches signals such as (CERR signal and the NCERR signal) which control the interrupts to the various CPUs in the computer system (see col. 11, lines 62-67).

As per claim 9:

Abdoo teaches a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11).

As per claim 10:

Abdoo in figure 1 teaches that the computer system comprising an EISA bus 42 is coupled through buffers 56 to a bus referred to as the X bus 60. A number of peripheral devices are coupled to the X bus 60, including a keyboard controller 62, a real time clock (RTC) 64, and an electrically erasable programmable read only memory (EEPROM) 66, (see col. 4, lines 44-54).

As per claims 14:

Abdoo substantially teaches or discloses a system includes an error detection and correction system (EDC) for detecting and correcting bit errors. In addition, if errors are caused by a faulty DRAM, the computer system determines the particular location identity of the failed DRAM module (see col. 1, lines 8-11). Abdoo further in figure 1 discloses the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block (a flag apparatus) referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22). Furthermore, Abdoo teaches signals such as (CERR signal and the NCERR signal) which controls the interrupts to the various CPUs in the computer system (see col. 11, lines 62-67).

As per claims 15 and 16:

Abdoo further in figure 1 discloses that the computer system (a data processing system) includes two CPU's (CPU0 20 and CPU1 22) (central processors unit), a memory controller (30), a main memory array (32) (a memory portion having storage units for storing data), a pair data buffers (SDBs) (44, 45) where in each of the buffers comprise error detection correction unit (see figure 2, element 82), (a memory for storing error detection/correction bits) connected to the memory array (32) and a logic block (a flag apparatus) referred to as the common system peripheral (CSP) (46) receives interrupt signals from the various peripheral I/O devices and

transmits these interrupt request signals to each of the CPU's (see col. 2, lines 56-67 and col. 3, lines 1-22).

As per claim 17:

Abdoo in figure 1 discloses that the computer system comprising an EISA bus 42 is coupled through buffers 56 to a bus referred to as the X bus 60. A number of peripheral devices are coupled to the X bus 60, including a keyboard controller 62, a real time clock (RTC) 64, and an electrically erasable programmable read only memory (EEPROM) 66, (see col. 4, lines 44-54).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Esaw T. Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8am-4PM…0.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EA/

/Esaw T Abraham/

Examiner, Art Unit 2112

06/25/08